IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): R.A. Corley et al.
Case: 1-1
Serial No.: 10/630,961
Filing Date: July 30, 2003
Group: 2609
Examiner: Mon Cheri S. Davenport

Title: Processor Configured for Efficient Processing of Single-Cell Protocol Data Units

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") hereby appeal the final rejection dated October 17, 2007 of claims 1-14 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on July 30, 2003 with claims 1-14, all of which remain pending. Claims 1, 13 and 14 are the independent claims.

Each of claims 1-14 stands rejected under 35 U.S.C. §102(b). Claims 1-14 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit. The processor is connectable to a second memory circuitry external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the processor recited in claim 1 are described in the specification at, for example, page 5, lines 1-19, with reference to FIG. 1. A processor (e.g., network processor 102) comprises controller circuitry (e.g., controller 120) and first memory circuitry (e.g., internal memory 104) internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor (e.g., from network 108) whether the given protocol data unit is a single-cell protocol data unit (see, e.g., page 5, lines 17-19, of the specification). The processor is connectable to a second memory circuitry (e.g., external memory 106) external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., single-cell storage portion 122, described at page 5, lines 13-15, of the specification), and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit

(e.g., multi-cell linked list storage portion 124, described at page 5, lines 15-17, of the specification).

Independent claim 13 is directed to a method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the method recited in claim 13 are described in the specification at, for example, page 7, line 6, to page 8, line 8, with reference to FIG. 3. A method (e.g., that shown in flow diagram 300) is suitable for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor (e.g., in step 302) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306); and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308).

Independent claim 14 is directed to a processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The instructions when executed in the processor implement the steps of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell

protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the medium recited in claim 14 are described in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3. A processor-readable medium contains processor-executable instructions (e.g., software code, as recited in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3) for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The instructions when executed in the processor implement the steps of determining for a given protocol data unit received by the processor (e.g., step 302 in FIG. 3) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304 in FIG. 3); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306 in FIG. 3); and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308 in FIG. 3).

The claimed invention provides a number of significant advantages over conventional arrangements. In an illustrative embodiment, single-cell PDUs are stored in an internal memory of the processor, thereby reducing the number of accesses to external memory. This results in improved processor performance and throughput. See also the specification at, for example, page 3, lines 9-13, and page 7, lines 6-13.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,278,834 (hereinafter "Mazzola").

ARGUMENT

Appellants initially note that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Appellants respectfully traverse the §102(b) rejection on the ground that the Mazzola reference fails to teach or suggest each and every limitation of claims 1-14 as alleged.

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to a second memory circuitry external to the processor. Illustrative embodiments of the claimed arrangements are described in the present specification at, for example, page 4, lines 22-28 (describing "an internal memory of the network processor" and "a memory external to the network processor"); page 5, lines 12-19 (with reference to FIG. 1); and page 8, lines 10-14 (with reference to FIG. 4).

The Examiner in formulating the §102(b) rejection argues that the limitations of claim 1 are met by the arrangement shown in FIG. 1 of Mazzola. More specifically, the Examiner argues that memory 14a and 14b are the recited first memory circuitry internal to the processor because memory 14a and memory 14b are used for internal functions of processor 12. See the Advisory Action at page 2, second paragraph, and the final Office Action at page 2, fourth paragraph.

Appellants respectfully disagree. As noted above, claim 1 is directed to a processor comprising first memory circuitry internal to the processor. Appellants respectfully submit that claim 1 therefore requires that the processor itself contain the recited first memory circuitry. See, e.g., MPEP 2111.03 (describing the transitional term "comprising" as "synonymous with 'including,' 'containing,' or 'characterized by'"). See also CIAS Inc. v. Alliance Gaming Corp., 504 F.3d 1356, 1360, 84 USPQ2d 1737, 1740 (Fed. Cir. 2007) ("In the patent claim context the term 'comprising' is well understood to mean 'including but not limited to.'"); id. at 1361, 84 USPQ2d 1737 at 1741 (quoting Robert A. Faber, Landis on Mechanics of Patent Claim Drafting

§2:5, 2-15 (5th ed. 2006) ("Other words, less often used, have been given the same meaning in patent claim interpretation as 'comprising': 'including,' 'having,' [and] 'containing'").

Appellants respectfully note that memory 14a and memory 14b each refer to areas within memory 14. See, for example, Mazzola at FIG. 1 and at column 3, lines 39-48. Mazzola expressly indicates that memory 14, and hence 14a and 14b, is not contained within processor 12. See, for example, Mazzola at FIG. 1 and at column 3, lines 13-15 ("Each end system node 10 has a processor 12 in communication with a memory 14"). Indeed, the Examiner concedes that memory 14 is not contained with processor 12 but rather is located "externally to the processor; the memory is connected via internal bus 13." See the Advisory Action at page 2, second paragraph; see also the final Office Action at page 2, fifth paragraph.

Furthermore, even if one accepts the Examiner's characterization of Mazzola's memory 14a and 14b as the recited first memory circuitry and memory 14c as the recited second memory circuitry, Appellants respectfully submit that Mazzola still fails to teach or suggest the limitation of claim 1 wherein information characterizing a given protocol data unit (PDU) is stored in the first memory circuitry if the given PDU is a single-cell PDU, and information characterizing the given PDU is stored in the second memory circuitry if the given PDU is not a single-cell PDU.

Rather than teaching the arrangement recited above, Mazzola instead teaches an arrangement wherein a single-cell PDU is stored within a single memory buffer and a multiple-cell PDU is stored in a linked list comprising multiple buffers. See, e.g., Mazzola at column 4, lines 3-25. However, whether a given PDU is a single-cell PDU is stored within a single memory buffer or a multiple-cell PDU stored in a linked list comprising multiple buffers, all memory buffers are allocated within buffer pool 14c (which, as discussed above, the Examiner characterizes as the recited second memory circuitry); see, e.g., Mazzola at column 3, lines 45-47; see also Mazzola at column 4, lines 3-11. Indeed, the Examiner concedes that buffer pool 14c stores single-cell PDUs; see the final Office Action at page 2, fifth and sixth paragraphs (Memory 14c "is the buffer pool from which memory buffer [sic] are allocated. . . . [T]he buffer contains a PDU big enough to be transmitted as [sic] single data unit."

Accordingly, Mazzola fails to teach or suggest the claimed arrangements in which information characterizing a given protocol data unit received by a processor is stored in first

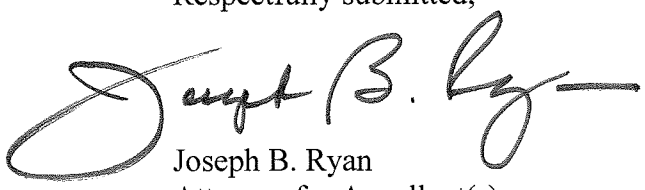
memory circuitry internal to the processor if the received protocol data unit is a single-cell protocol data unit, and is stored in second memory circuitry external to the processor if the received protocol data unit is not a single-cell protocol data unit. Rather, by using a memory 14 that is external to processor 12 to store all protocol data units, regardless of whether or not such protocol data units are single-cell units or multi-cell units, Mazzola appears to suffer from the very problems identified by Appellants at page 2, lines 1-13 of the specification.

Independent claims 13 and 14 include limitations similar to those of claim 1, and are believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-12 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the above, Appellants believe that claims 1-14 are in condition for allowance, and respectfully request the withdrawal of the §102(b) rejection.

Respectfully submitted,



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CLAIMS APPENDIX

1. A processor comprising:

controller circuitry configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; and

first memory circuitry internal to the processor;

the processor being connectable to second memory circuitry external to the processor;

wherein information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

wherein information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

2. The processor of claim 1 wherein the protocol data unit comprises a packet.

3. The processor of claim 1 wherein the single-cell protocol data unit comprises a protocol data unit having a size less than or substantially equal to that of a cell-based processing unit of a switch fabric associated with the processor.

4. The processor of claim 1 wherein the information characterizing the given protocol data unit comprises at least one block descriptor.

5. The processor of claim 4 wherein the block descriptor is associated with a particular data block of the given protocol data unit.

6. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the first memory circuitry without requiring utilization of a linked list data structure.

7. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the second memory circuitry utilizing a linked list data structure.

8. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the protocol data unit between a network and a switch fabric.

9. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a queuing and dispatch buffer memory of the processor.

10. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a PDU buffer memory of the processor.

11. The processor of claim 1 wherein the processor comprises a network processor.

12. The processor of claim 1 wherein the processor is configured as an integrated circuit.

13. A method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the method comprising the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

14. A processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the instructions when executed in the processor implementing the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None